AMENDMENTS TO THE CLAIMS

1. – 58. (Cancelled).

59. (Original) A processor system comprising:

a processor; and

memory device coupled to said processor, said processor and memory device residing on a common substrate, said substrate having a through-hole, said substrate further comprising a top side and a bottom side with multi-layer structure interposed on both sides of said substrate and passing through said through-hole, said multi-layer structure comprising:

a conductive plane; and

a signal wiring layer, said conductive plane and said signal wiring layer having an insulating layer interposed between them.

60. (Original) The processor system of claim 59, wherein said conductive plane comprises a first ground plane.

61. (Original) The processor system of claim 60, wherein said first ground plane is at least 3 μm thick.

62. (Original) The processor system of claim 60, wherein the thickness of said first ground plane is less than or equal to 5 μm.

63. (Original) The processor system of claim 59, wherein said conductive plane comprises a power supply distribution plane.

64. (Original) The processor system of claim 59, wherein said conductive plane comprises a copper plane.

65. (Original) The processor system of claim 59, wherein said conductive plane comprises an aluminum plane.

66. (Original) The processor system of claim 59, wherein said multi-layer structure further comprises a first insulating layer provided on the side said multi-layer structure directly adjacent to said substrate.

67. (Original) The processor system of claim 66, wherein said first insulating layer comprises a silicon dioxide layer.

68. (Original) The processor system of claim 67, wherein the thickness of said silicon dioxide layer is 0.1 to 0.5μm.

69. (Original) The processor system of claim 66, wherein said conductive plane is deposited over said first insulating layer.

70. (Original) The processor system of claim 59, wherein said insulating layer comprises a second insulating layer formed over said conductive plane.

71. (Original) The processor system of claim 59, wherein said multi-layer structure further comprises a third insulating layer formed over said signal wiring layer.

72. (Original) The processor system of claim 71, wherein said multi-layer structure further comprises a second conductive plane formed over said third insulating layer.

73. (Original) The processor system of claim 70, wherein said second insulating layer comprises silicon dioxide.

74. (Original) The processor system of claim 70, where the thickness of said second insulating is 0.5 to 4.0μm.

75. (Original) The processor system of claim 59, wherein said signal wiring layer comprises at least one signal line.

76. (Original) The processor system of claim 75, wherein said at least one signal line is 6 to 10 μm wide.

77. (Original) The processor system of claim 71, wherein said third insulating layer comprises a silicon dioxide layer.

78. (Original) The processor system of claim 72, wherein the thickness of said second conductive plane is 3 μm to 5 μm.

79. (Original) The processor system of claim 75, wherein said at least one signal line is terminated at a bond pad.

80. (Original) The processor system of claim 70, wherein said second insulating layer comprises a polyimide layer.

81. (Original) The processor system of claim 71, wherein said third insulating layer comprises a silicon dioxide layer.

82. (Original) The processor system of claim 71, wherein said third insulating layer comprises a polyimide layer.

83. (Original) The processor system of claim 72, wherein said second conductive plane comprises a ground plane.

84. (Original) The processor system of claim 72, wherein said second conductive plane comprises a power supply distribution plane.

85. (Original) The processor system of claim 72, wherein said multi-layer structure further comprises a fourth insulating layer formed over said second conductive plane.

86. – 131. (Cancelled).